DATA STORAGE SYSTEM PACKER/UNPACKER
Jeffrey S. Kinne
EMC2-144PUS

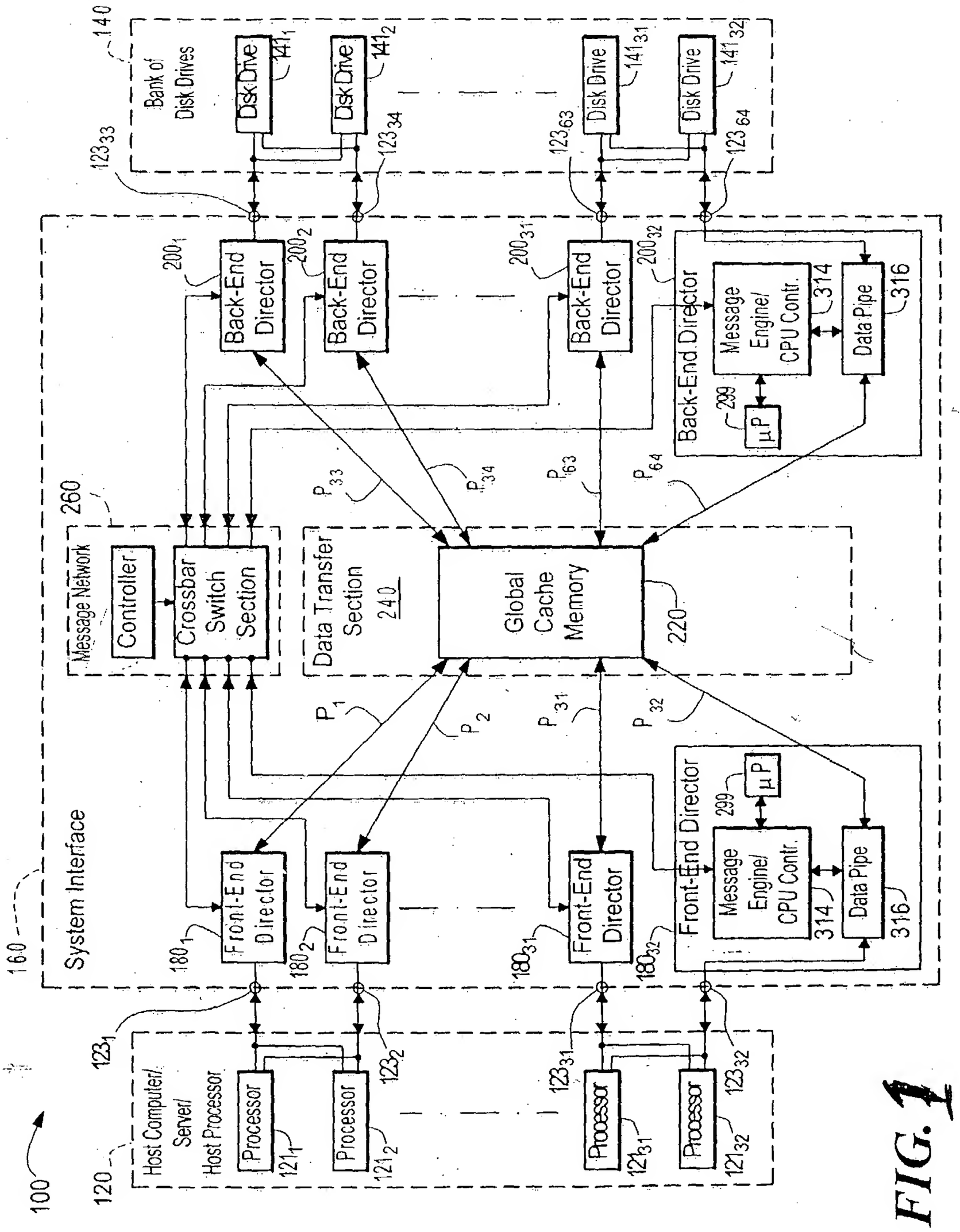


FIG. 1

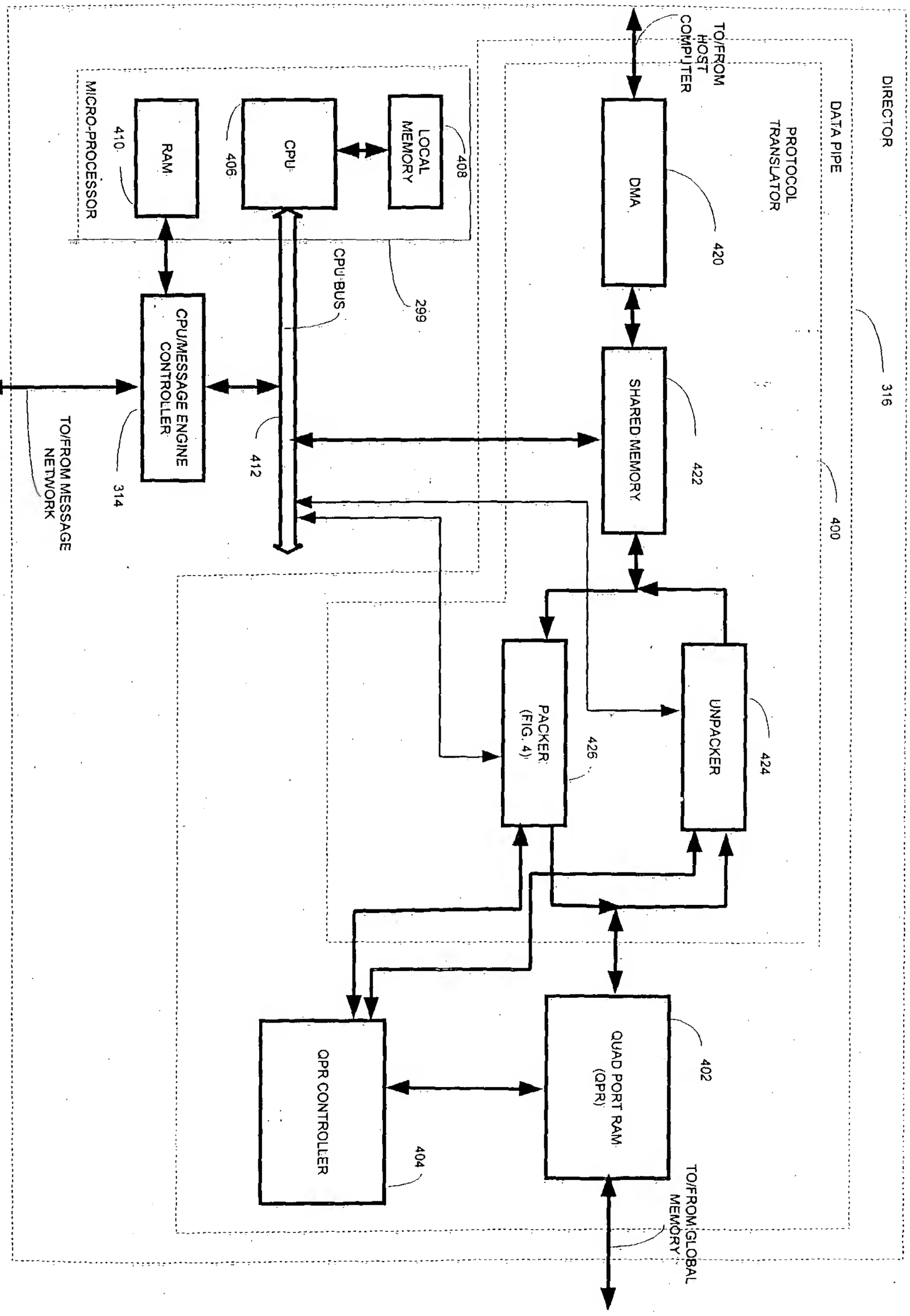
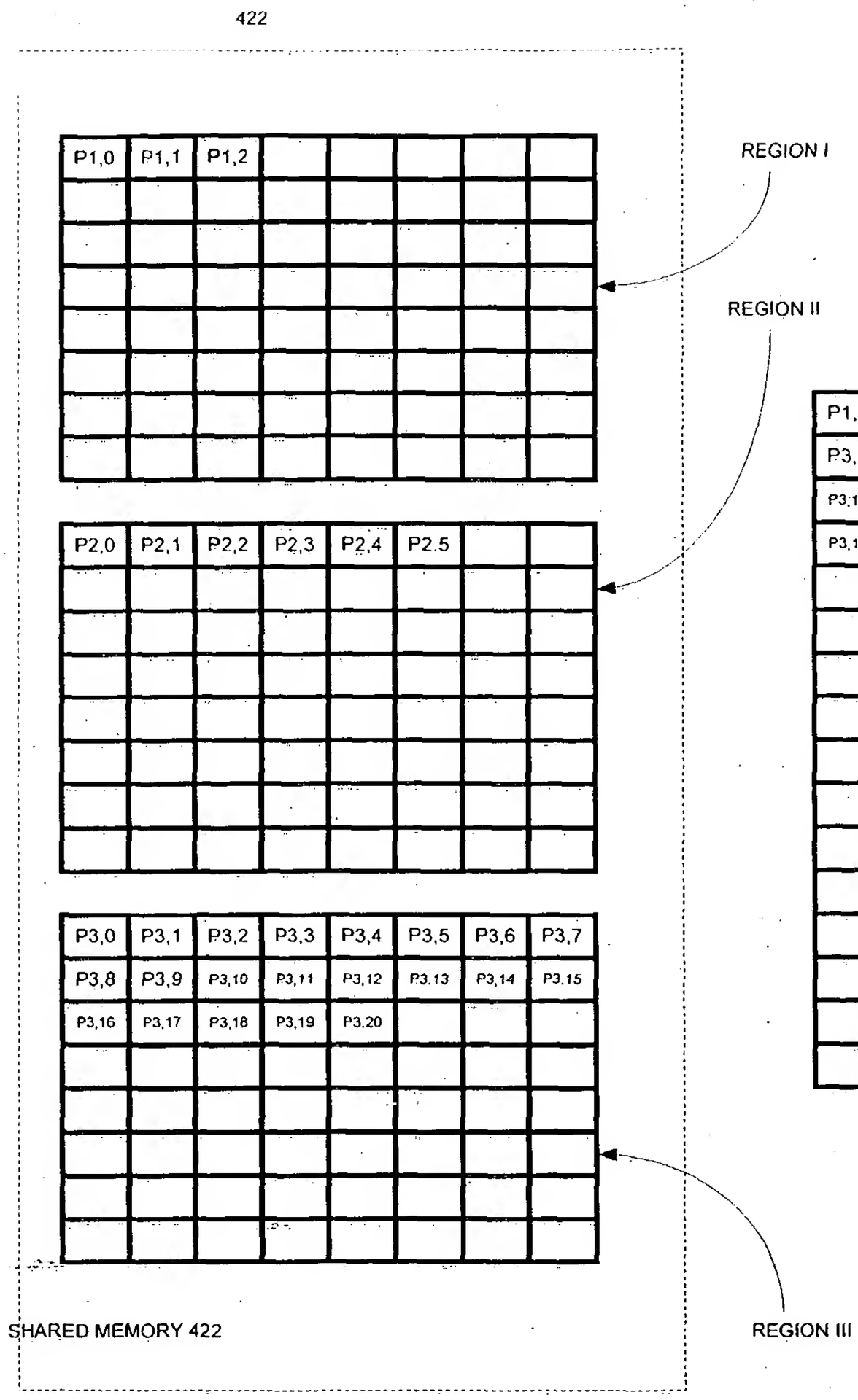

DIRECTOR
316
DATA PIPE
400
PROTOCOL TRANSLATOR
TO/FROM HOST COMPUTER
DMA
420
SHARED MEMORY
422
UNPACKER
424
PACKER (FIG. 4)
426
MICRO-PROCESSOR
RAM
410
CPU
406
LOCAL MEMORY
408
CPU BUS
299
CPU/MESSAGE ENGINE CONTROLLER
314
412
TO/FROM MESSAGE NETWORK
QUAD PORT RAM (QPR)
402
QPR CONTROLLER
404
TO/FROM GLOBAL MEMORY

FIG. 2

FIG. 3


422
P1,0 P1,1 P1,2
REGION I
REGION II
GLOBAL CACHE MEMORY 220
P1,1 P1,2 P2,1 P2,2 P2,3 P2,4 P2,5 P3,1
P3,2 P3,3 P3,4 P3,5 P3,6 P3,7 P3,8 P3,9
P3,10 P3,11 P3,12 P3,13 P3,14 P3,15 P3,16 P3,17
P3,18 P3,19 P3,20
P2,0 P2,1 P2,2 P2,3 P2,4 P2.5
P3,0 P3,1 P3,2 P3,3 P3,4 P3,5 P3,6 P3,7
P3,8 P3,9 P3,10 P3,11 P3,12 P3,13 P3,14 P3,15
P3,16 P3,17 P3,18 P3,19 P3,20
SHARED MEMORY 422
REGION III

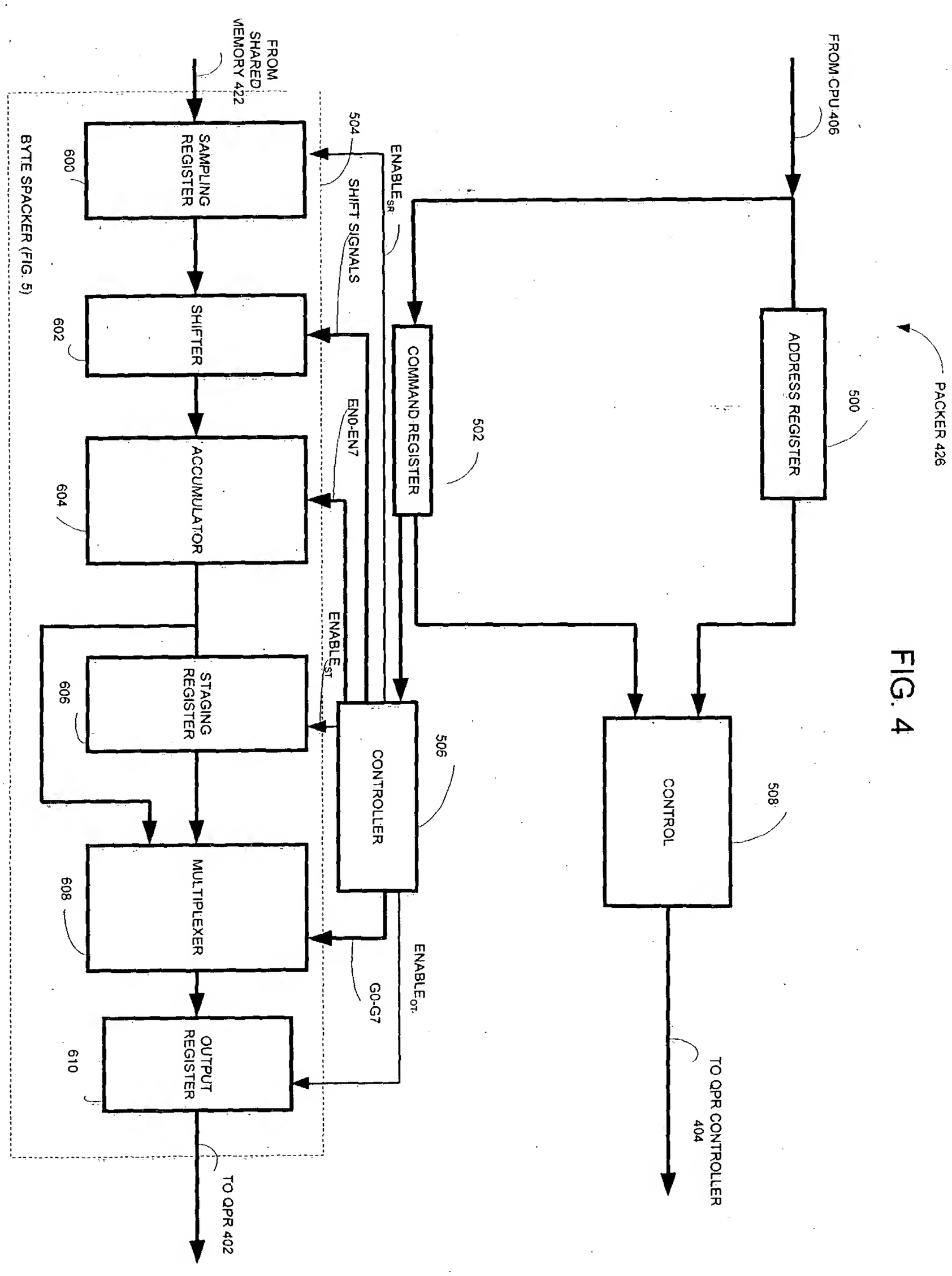
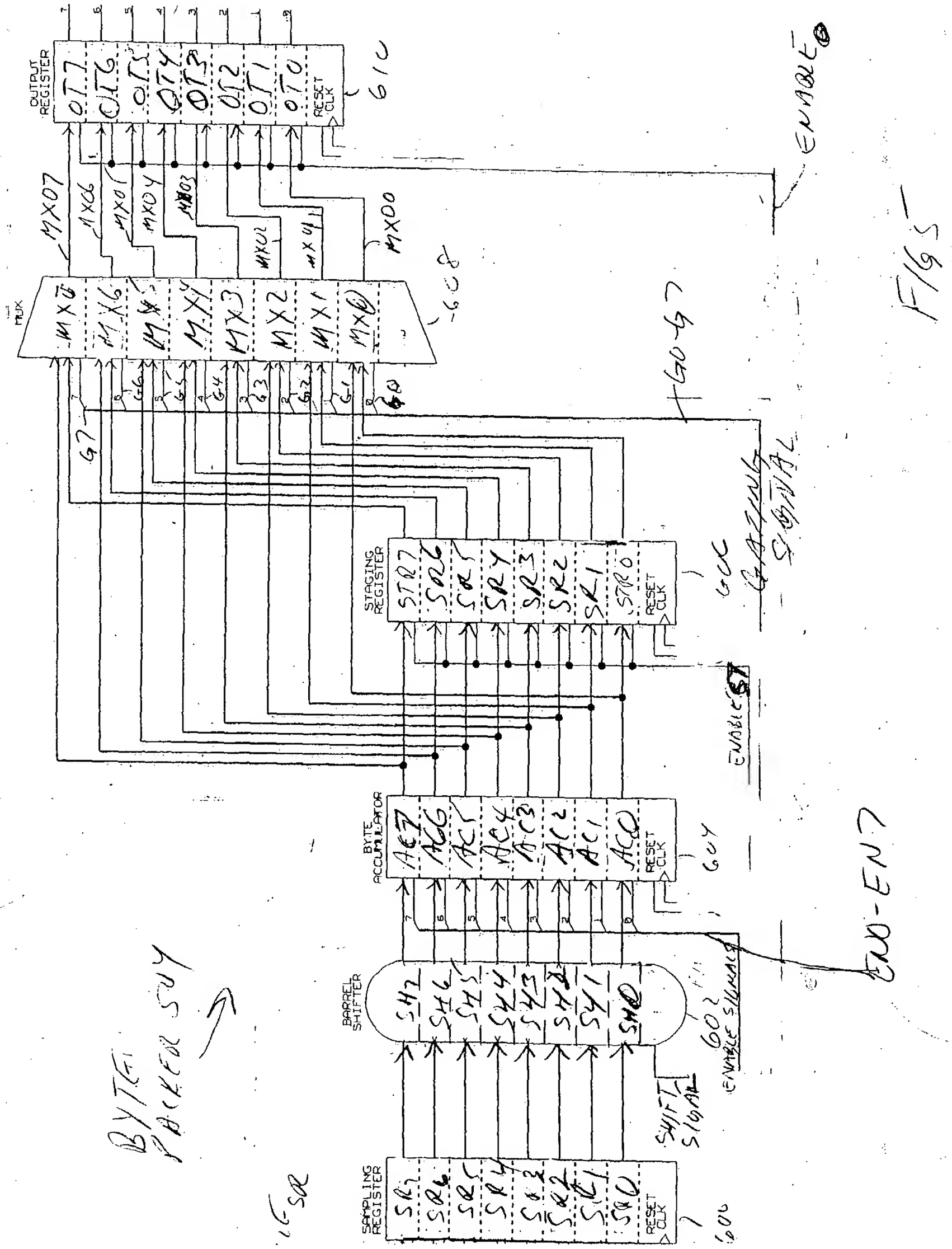

PACKER 426
FROM CPU 406
ADDRESS REGISTER
500
COMMAND REGISTER
502
CONTROL
508
TO QPR CONTROLLER 404
FROM SHARED MEMORY 422
BYTE SPACKER (FIG. 5)
SAMPLING REGISTER
600
SHIFTER
602
ACCUMULATOR
604
STAGING REGISTER
606
MULTIPLEXER
608
OUTPUT REGISTER
610
CONTROLLER
506
504
SHIFT SIGNALS
ENABLE$_{SR}$
EN0-EN7
ENABLE$_{ST}$
G0-G7
ENABLE$_{OT}$
TO QPR 402

FIG. 4


OUTPUT REGISTER
RESET CLK
MUX
STAGING REGISTER
BYTE ACCUMULATOR
BARREL SHIFTER
SAMPLING REGISTER
ENABLE
SHIFT SIGNAL
BYTE PACKER SM

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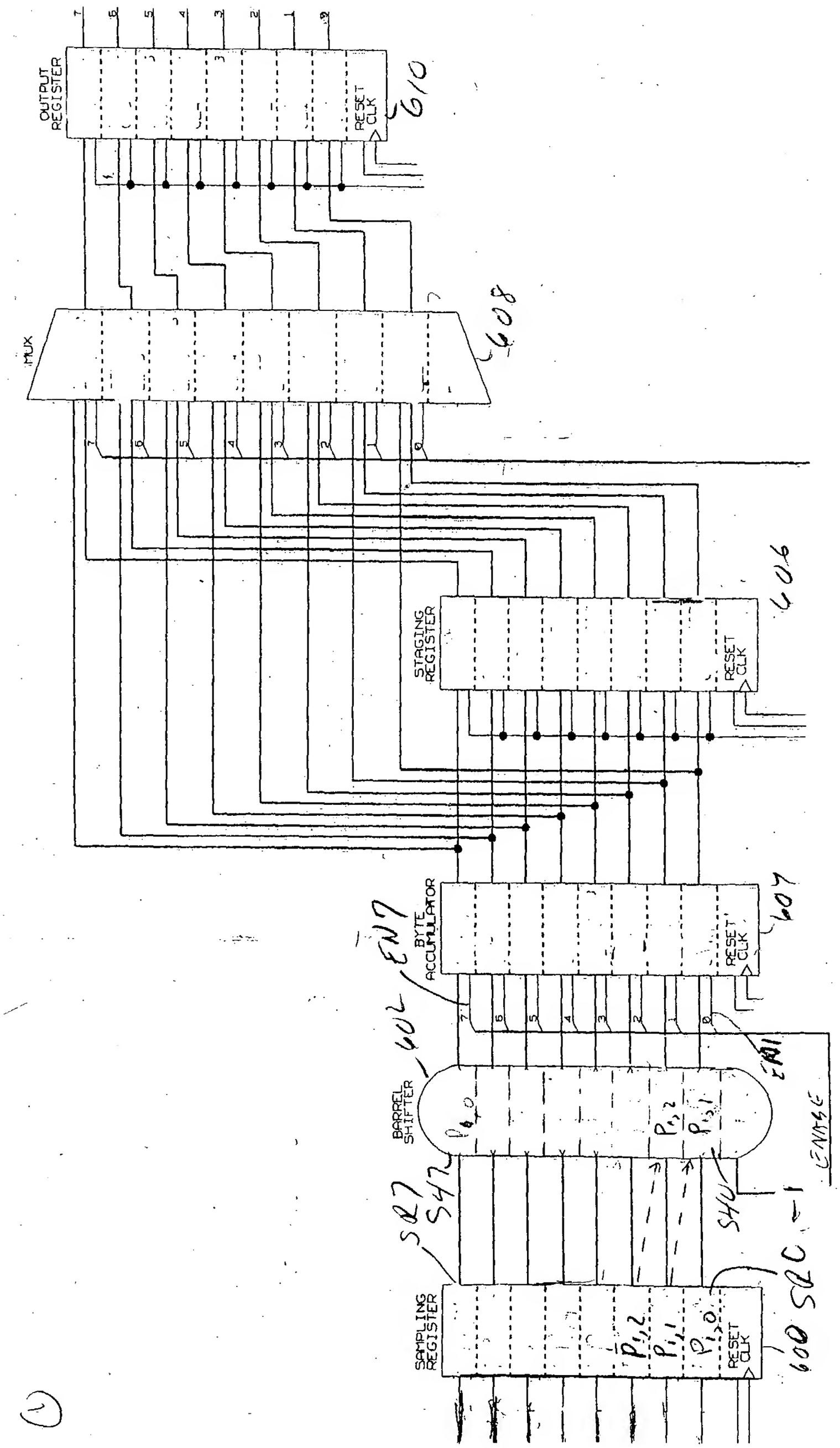


FIG 6A

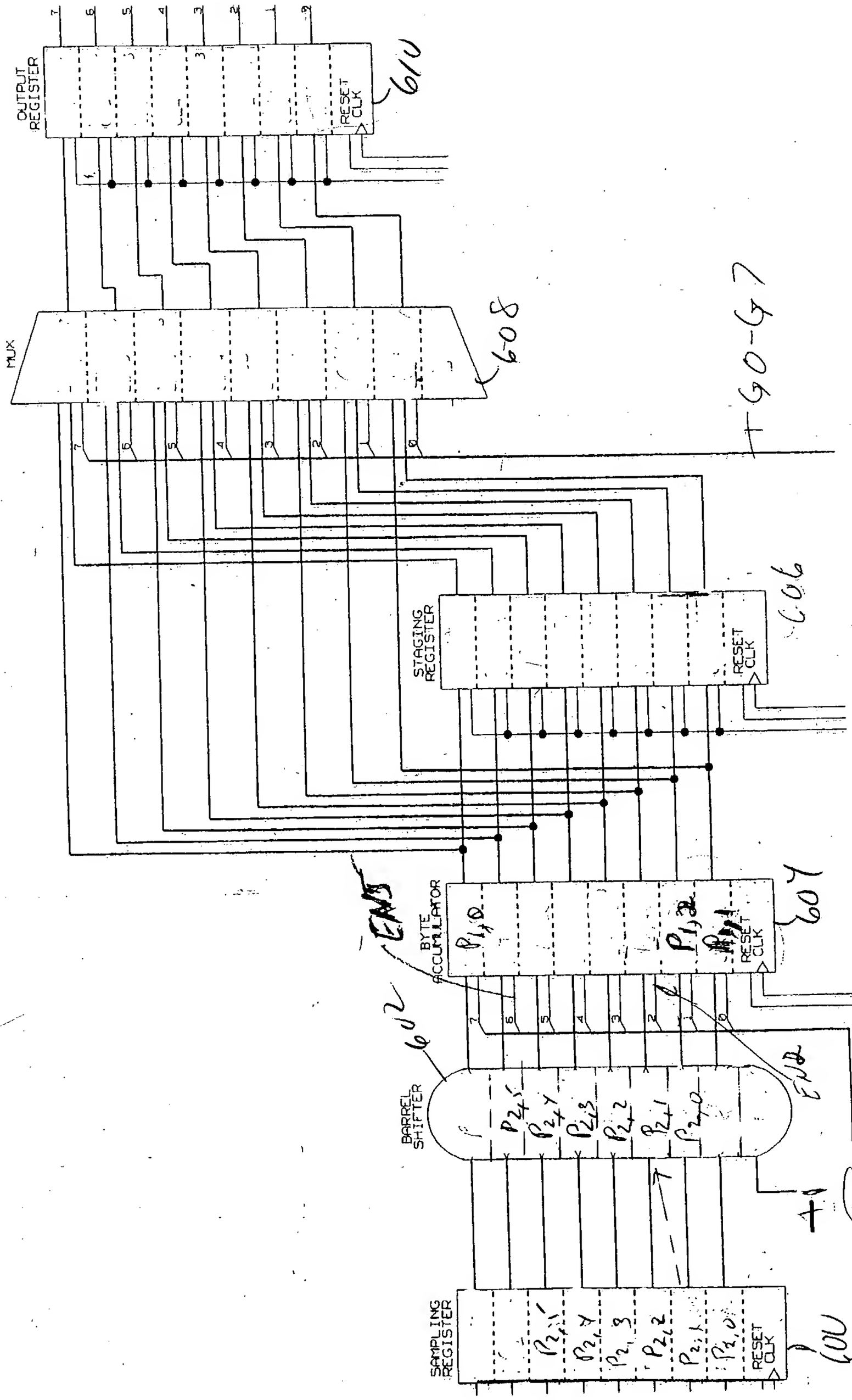
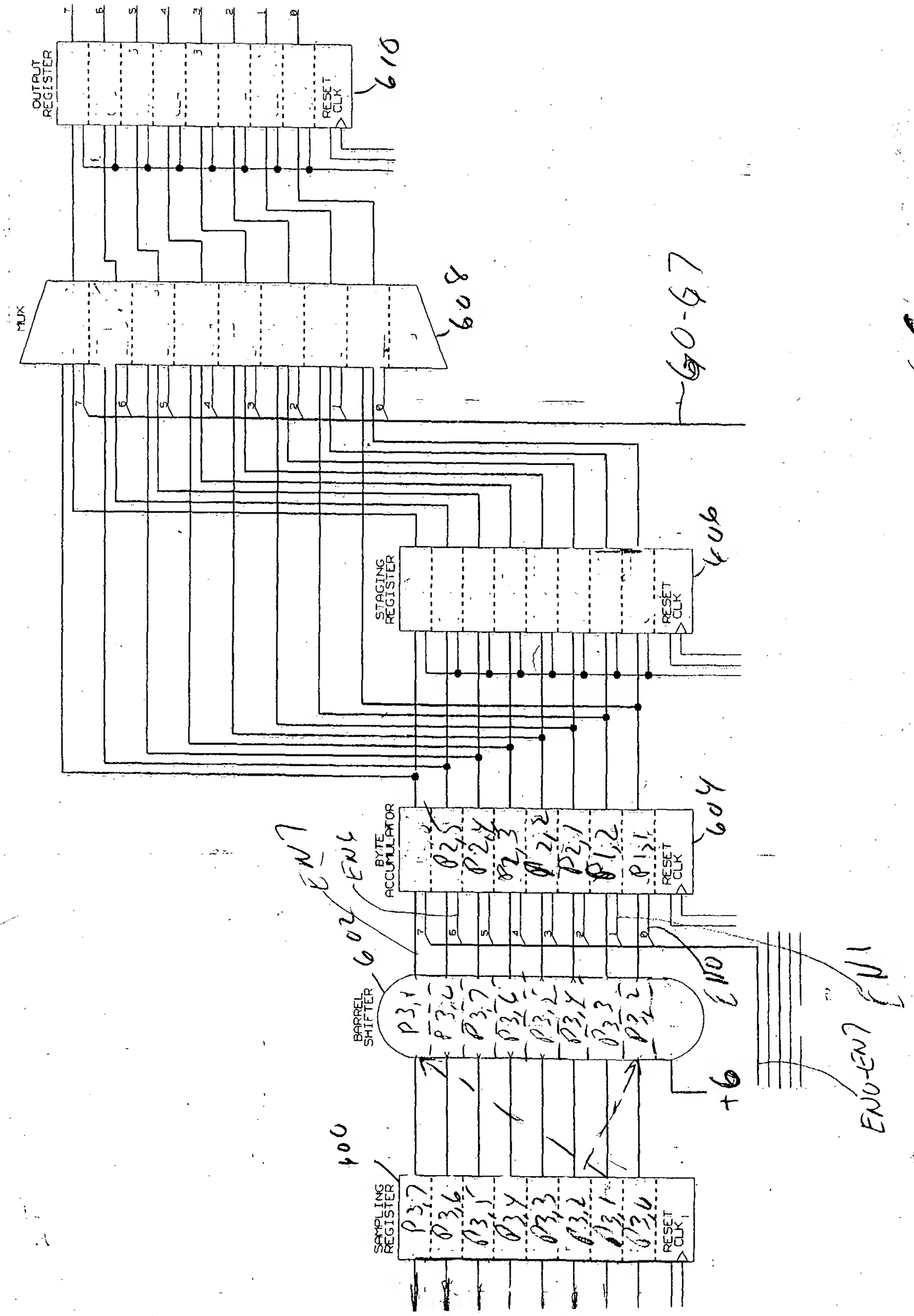
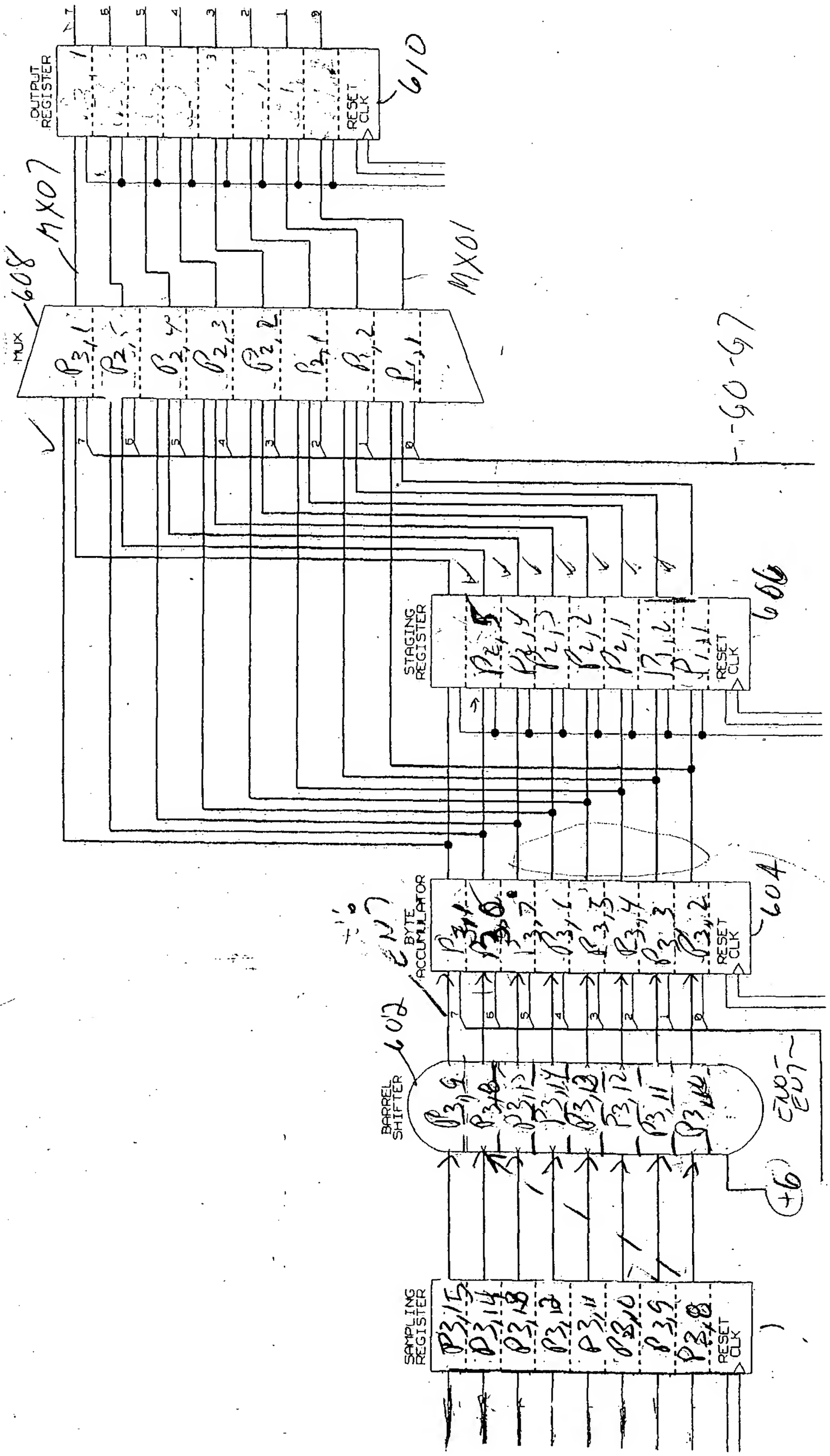
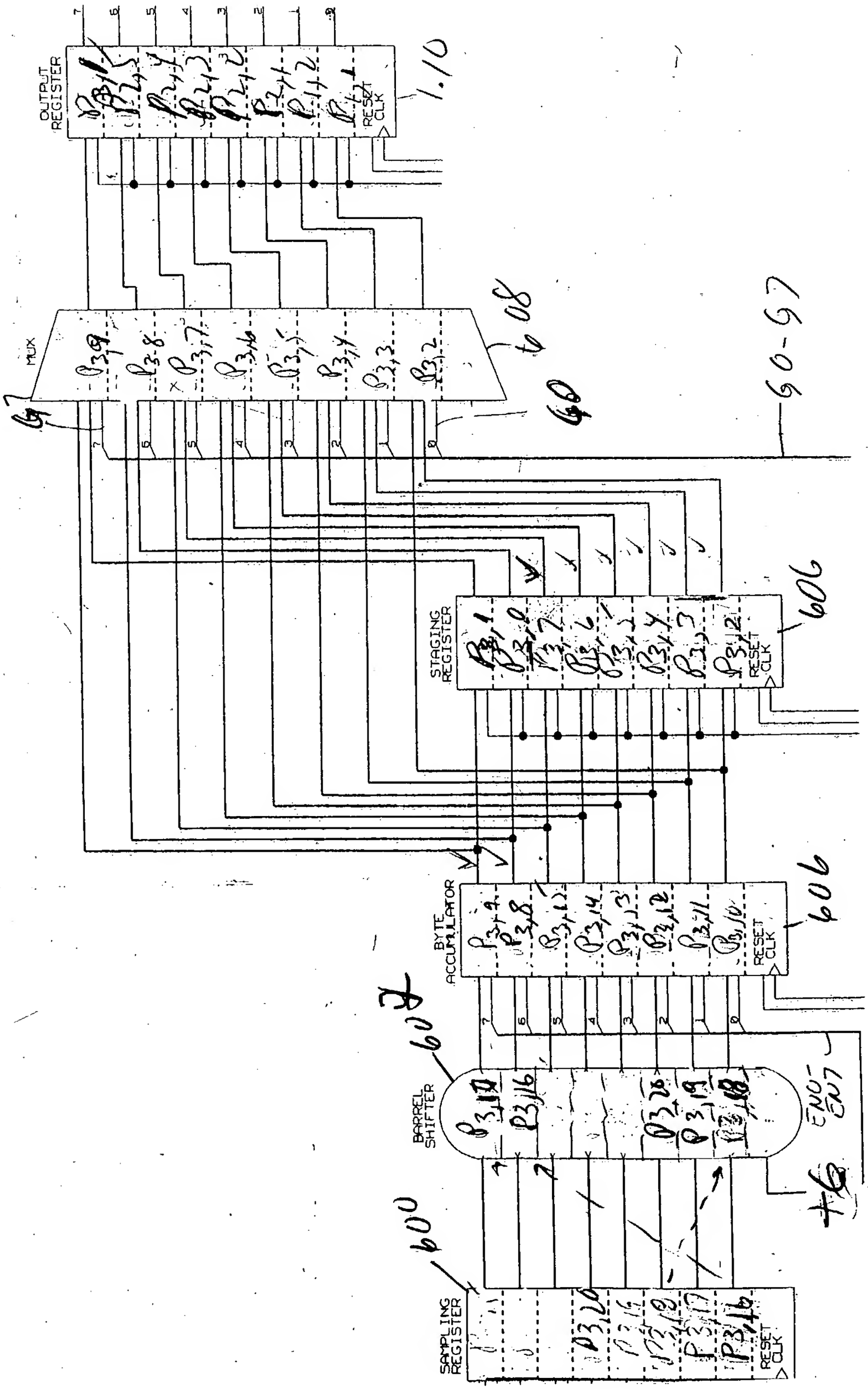

OUTPUT REGISTER
RESET CLK
610
MUX
608
STAGING REGISTER
606
BYTE ACCUMULATOR
607
BARREL SHIFTER
602
SAMPLING REGISTER
RESET CLK
600
EN 0 - EN 7

Fig. 6B


OUTPUT REGISTER
RESET CLK
MUX
STAGING REGISTER
RESET CLK
BYTE ACCUMULATOR
RESET CLK
BARREL SHIFTER
SAMPLING REGISTER
RESET CLK


OUTPUT REGISTER
RESET CLK
610
MUX
608
MX07
MX01
STAGING REGISTER
606
BYTE ACCUMULATOR
604
BARREL SHIFTER
602
SAMPLING REGISTER
RESET CLK


OUTPUT REGISTER
RESET
CLK
MUX
STAGING REGISTER
BYTE ACCUMULATOR
BARREL SHIFTER
SAMPLING REGISTER
RESET
CLK

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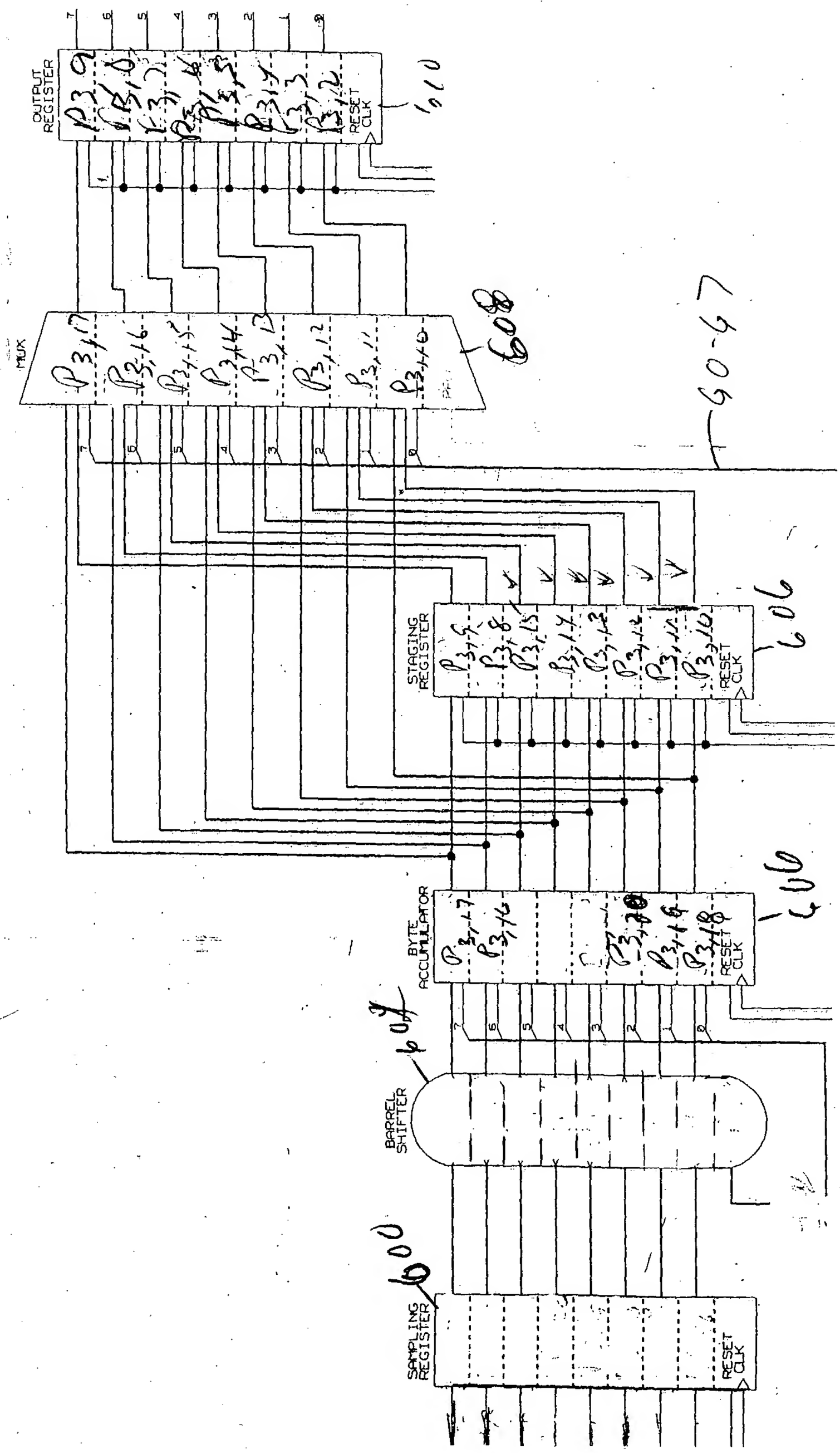

Fig. 6

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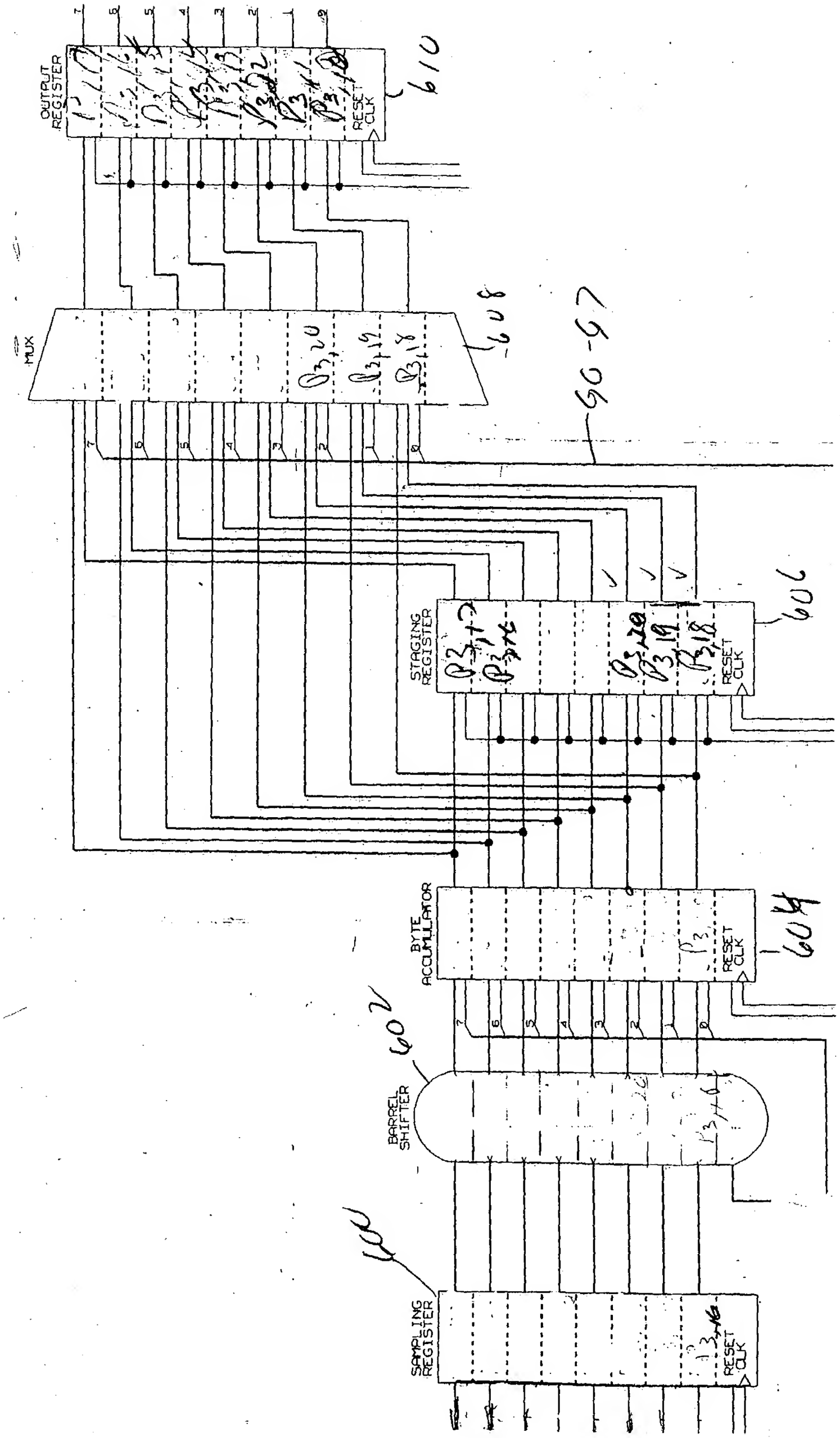


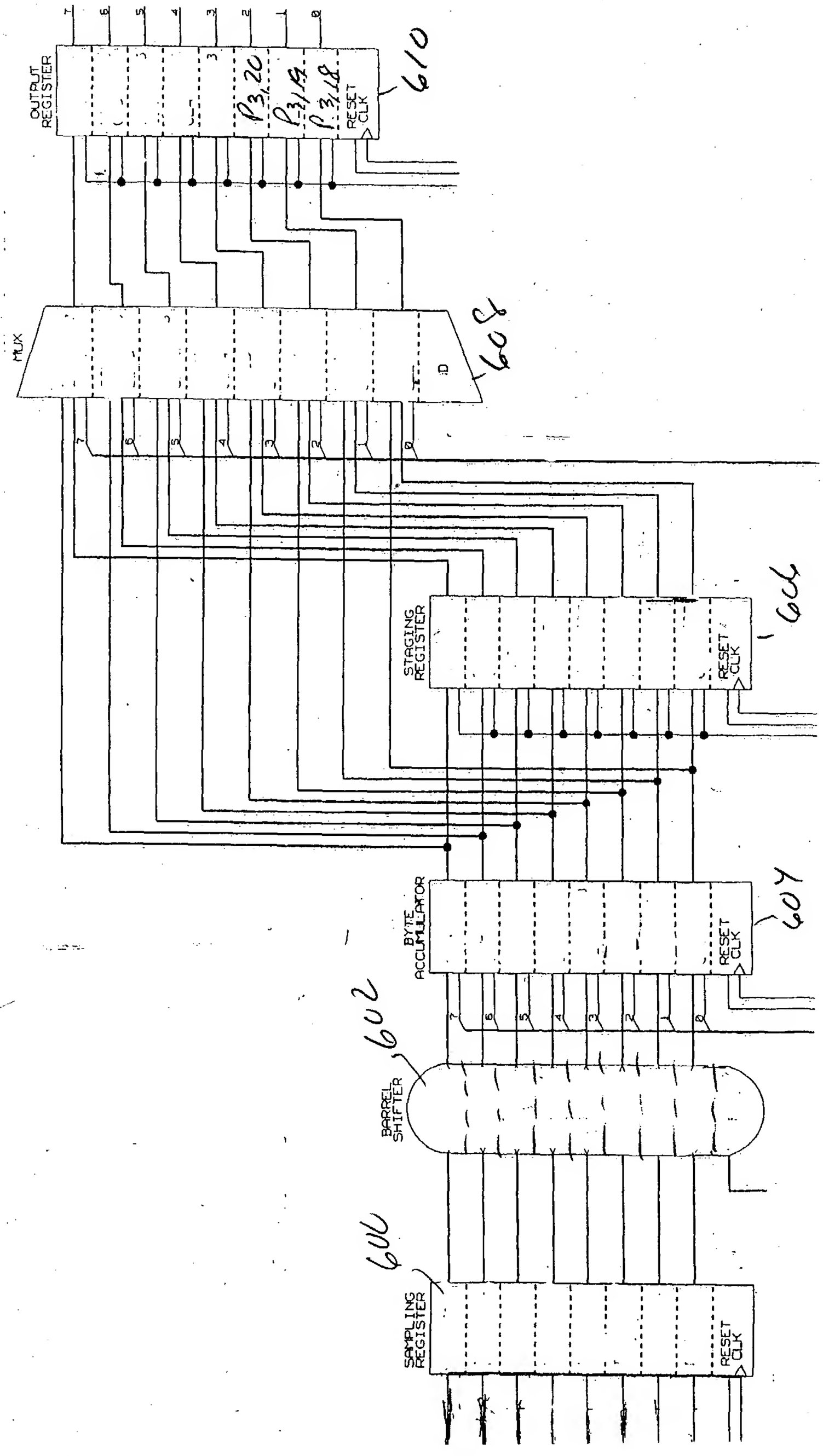
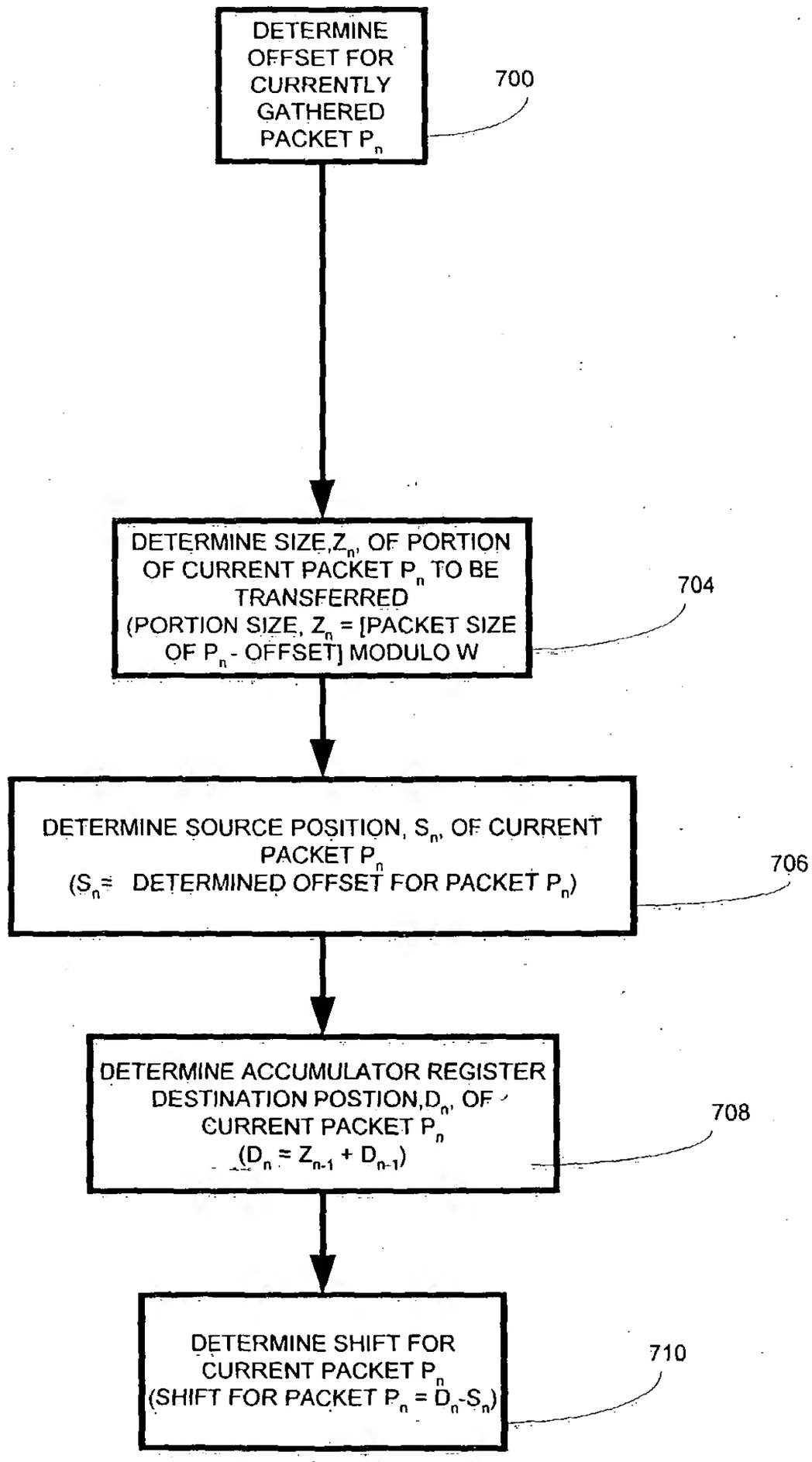

OUTPUT REGISTER
RESET CLK
610
MUX
D
608
STAGING REGISTER
606
BYTE ACCUMULATOR
604
BARREL SHIFTER
602
SAMPLING REGISTER

FIG 6H

FIG. 7


DETERMINE OFFSET FOR CURRENTLY GATHERED PACKET P_n
700
DETERMINE SIZE, Z_n, OF PORTION OF CURRENT PACKET P_n TO BE TRANSFERRED (PORTION SIZE, Z_n = [PACKET SIZE OF P_n - OFFSET] MODULO W
704
DETERMINE SOURCE POSITION, S_n, OF CURRENT PACKET P_n (S_n= DETERMINED OFFSET FOR PACKET P_n)
706
DETERMINE ACCUMULATOR REGISTER DESTINATION POSTION, D_n, OF CURRENT PACKET P_n ($D_n = Z_{n-1} + D_{n-1}$)
708
DETERMINE SHIFT FOR CURRENT PACKET P_n (SHIFT FOR PACKET $P_n = D_n - S_n$)
710

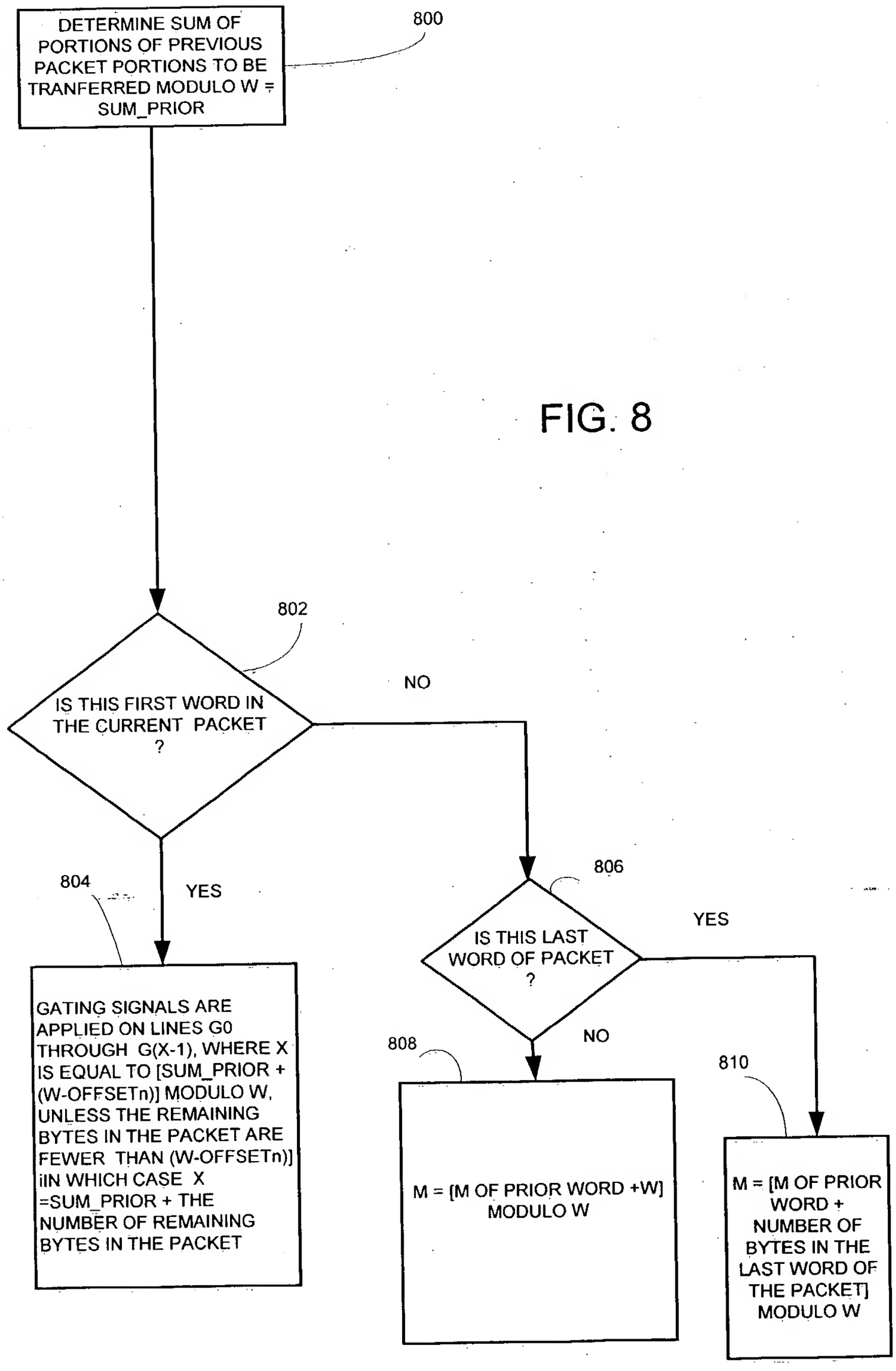

DETERMINE SUM OF PORTIONS OF PREVIOUS PACKET PORTIONS TO BE TRANFERRED MODULO W = SUM_PRIOR
800
802
IS THIS FIRST WORD IN THE CURRENT PACKET ?
NO
804
YES
GATING SIGNALS ARE APPLIED ON LINES G0 THROUGH G(X-1), WHERE X IS EQUAL TO [SUM_PRIOR + (W-OFFSETn)] MODULO W, UNLESS THE REMAINING BYTES IN THE PACKET ARE FEWER THAN (W-OFFSETn)] iIN WHICH CASE X =SUM_PRIOR + THE NUMBER OF REMAINING BYTES IN THE PACKET
806
IS THIS LAST WORD OF PACKET ?
YES
NO
808
M = [M OF PRIOR WORD +W] MODULO W
810
M = [M OF PRIOR WORD + NUMBER OF BYTES IN THE LAST WORD OF THE PACKET] MODULO W

FIG. 8

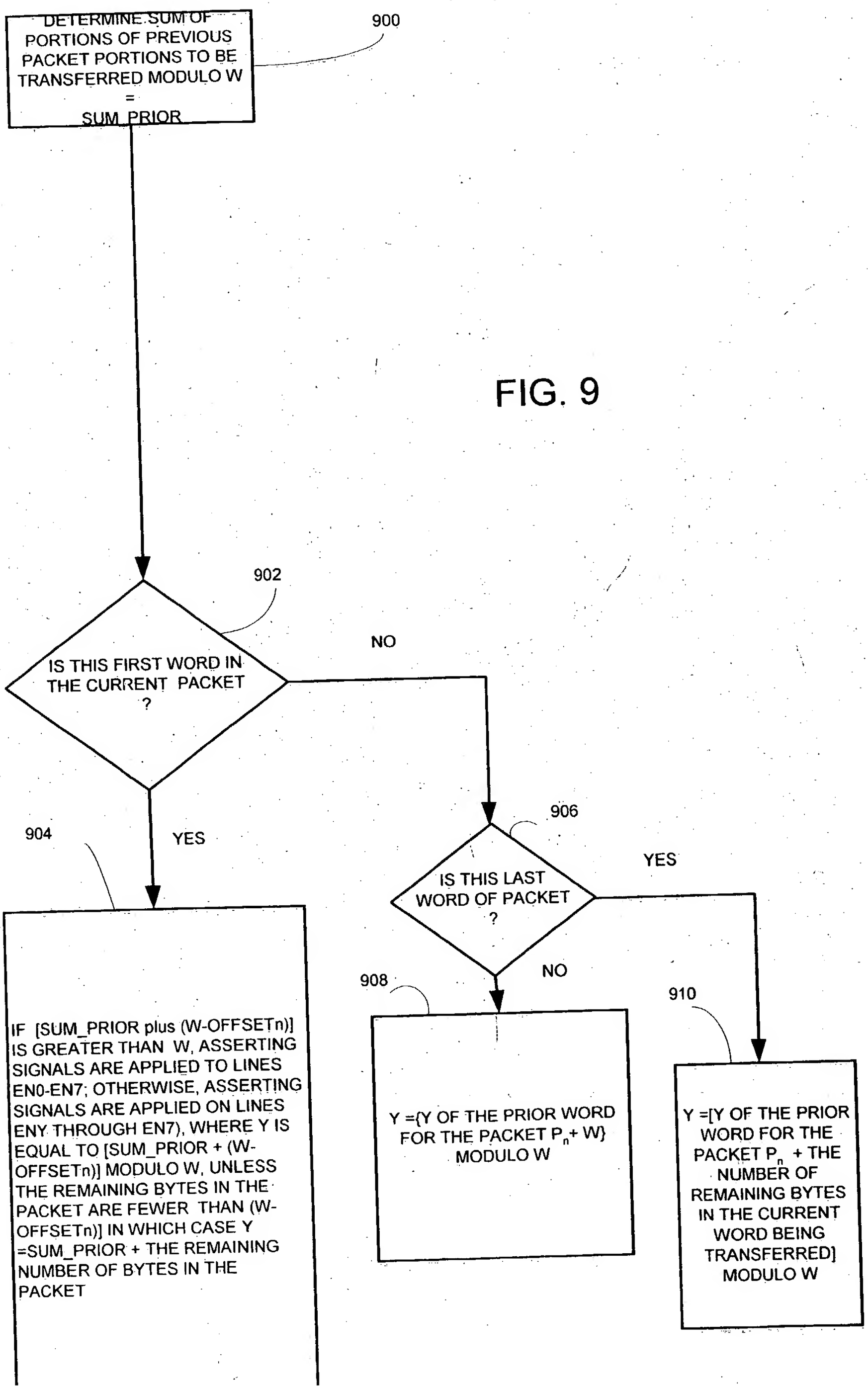

DETERMINE SUM OF PORTIONS OF PREVIOUS PACKET PORTIONS TO BE TRANSFERRED MODULO W = SUM_PRIOR
900
IS THIS FIRST WORD IN THE CURRENT PACKET ?
902
NO
YES
904
IF [SUM_PRIOR plus (W-OFFSETn)] IS GREATER THAN W, ASSERTING SIGNALS ARE APPLIED TO LINES EN0-EN7; OTHERWISE, ASSERTING SIGNALS ARE APPLIED ON LINES ENY THROUGH EN7), WHERE Y IS EQUAL TO [SUM_PRIOR + (W-OFFSETn)] MODULO W, UNLESS THE REMAINING BYTES IN THE PACKET ARE FEWER THAN (W-OFFSETn)] IN WHICH CASE Y =SUM_PRIOR + THE REMAINING NUMBER OF BYTES IN THE PACKET
IS THIS LAST WORD OF PACKET ?
906
YES
NO
908
Y ={Y OF THE PRIOR WORD FOR THE PACKET P_n+ W} MODULO W
910
Y =[Y OF THE PRIOR WORD FOR THE PACKET P_n + THE NUMBER OF REMAINING BYTES IN THE CURRENT WORD BEING TRANSFERRED] MODULO W

FIG. 9

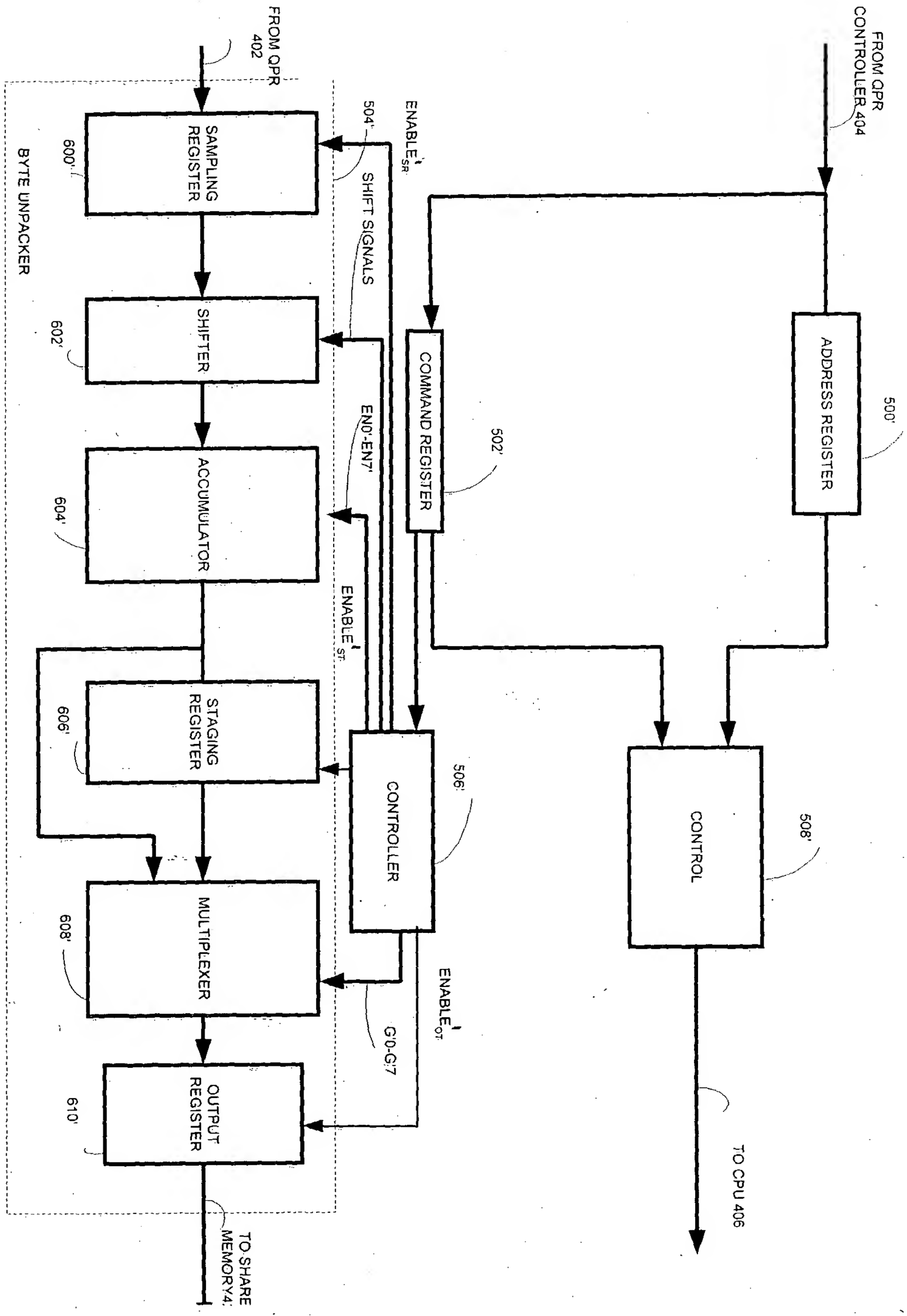
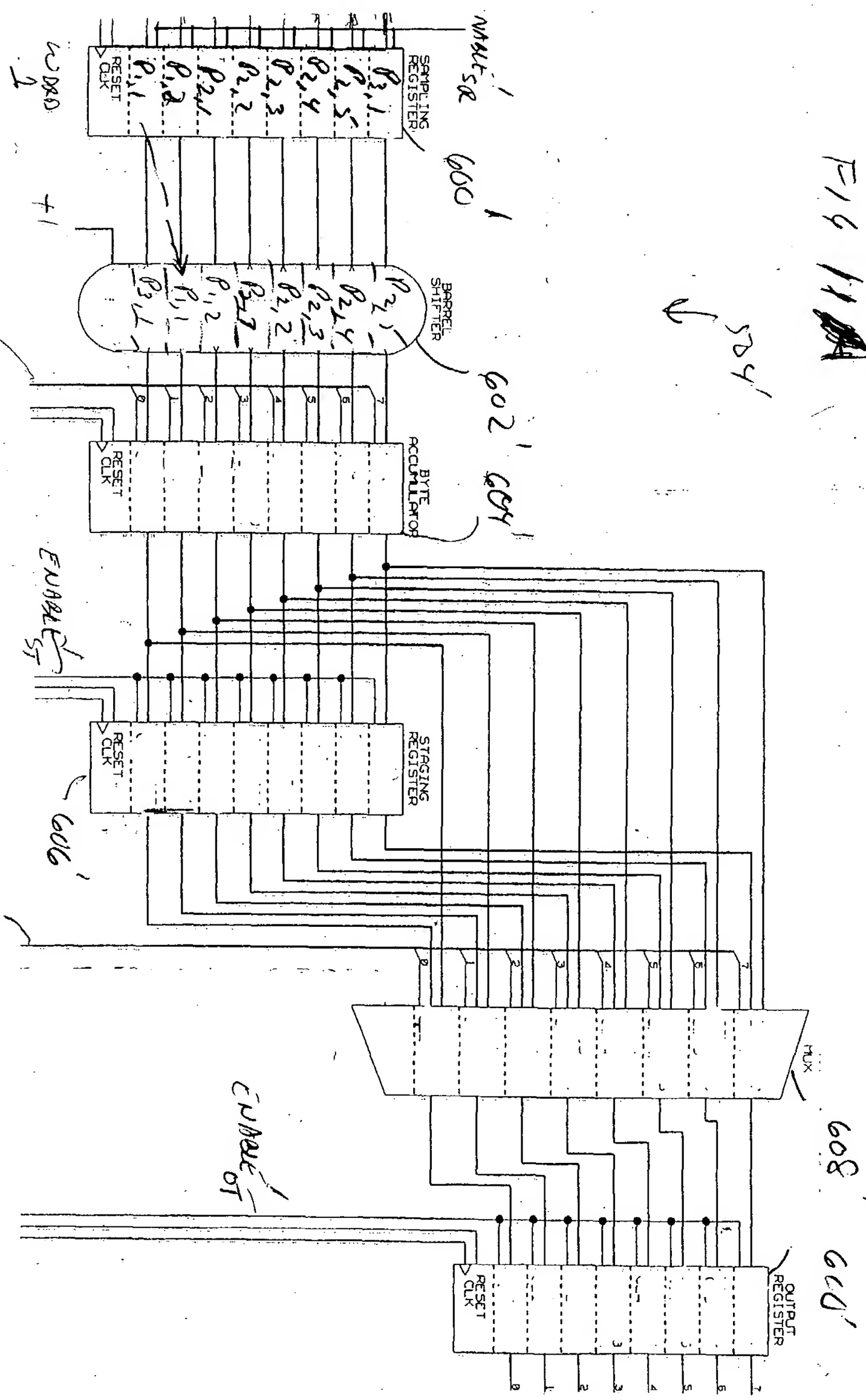
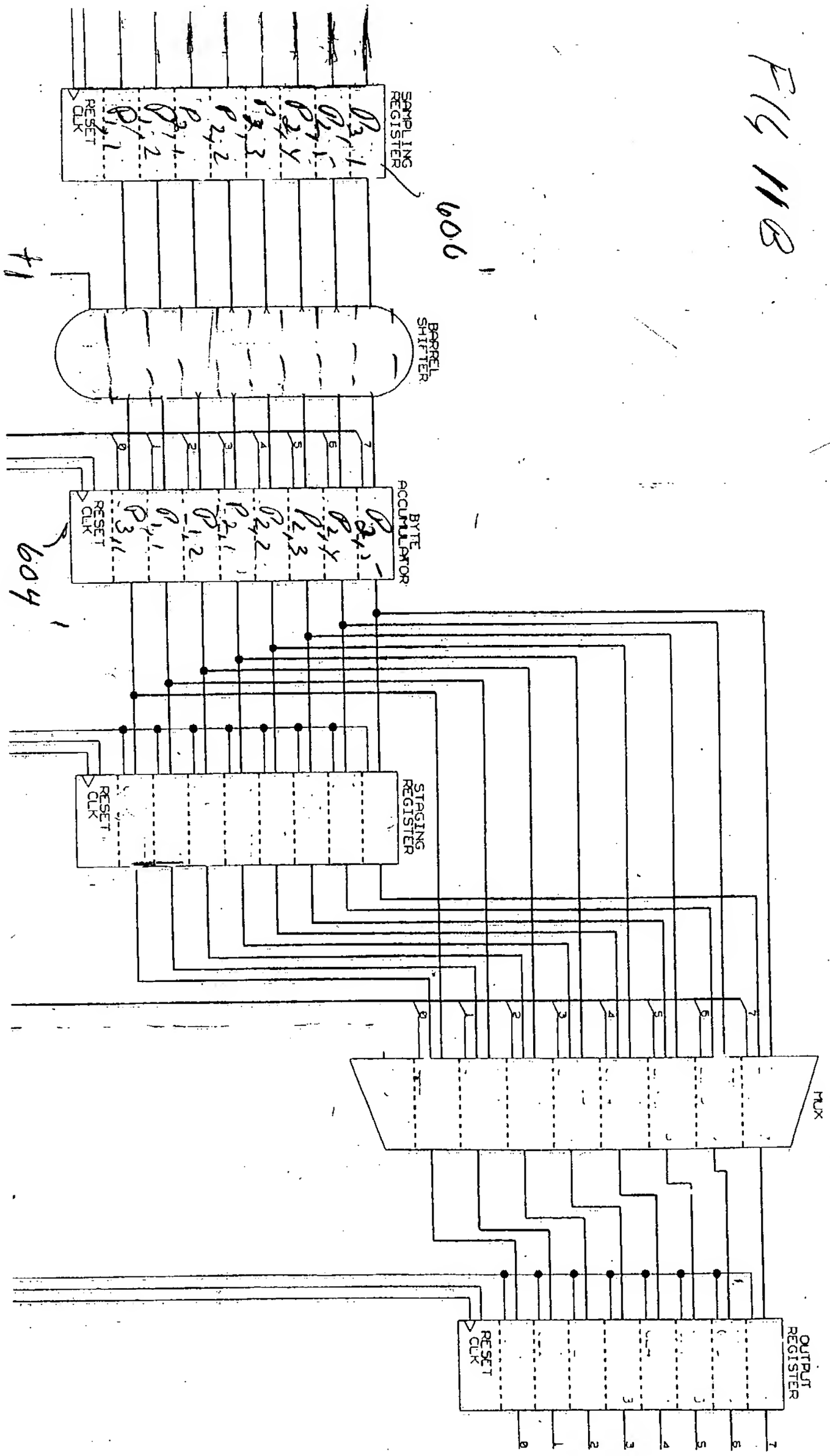

FROM QPR 402
BYTE UNPACKER
SAMPLING REGISTER
600'
SHIFTER
602'
ACCUMULATOR
604'
STAGING REGISTER
606'
MULTIPLEXER
608'
OUTPUT REGISTER
610'
TO SHARE MEMORY 410
504'
ENABLE'SR
SHIFT SIGNALS
EN0'-EN7'
ENABLE'ST
COMMAND REGISTER
502'
CONTROLLER
506'
ENABLE'OT
G'0-G'7
FROM QPR CONTROLLER 404
ADDRESS REGISTER
500'
CONTROL
508'
TO CPU 406
UNPACKER 424

FIG. 10


RESET CLK
SAMPLING REGISTER
BARREL SHIFTER
BYTE ACCUMULATOR
STAGING REGISTER
MUX
OUTPUT REGISTER


SAMPLING REGISTER
RESET CLK
606
BARREL SHIFTER
BYTE ACCUMULATOR
604
STAGING REGISTER
MUX
OUTPUT REGISTER

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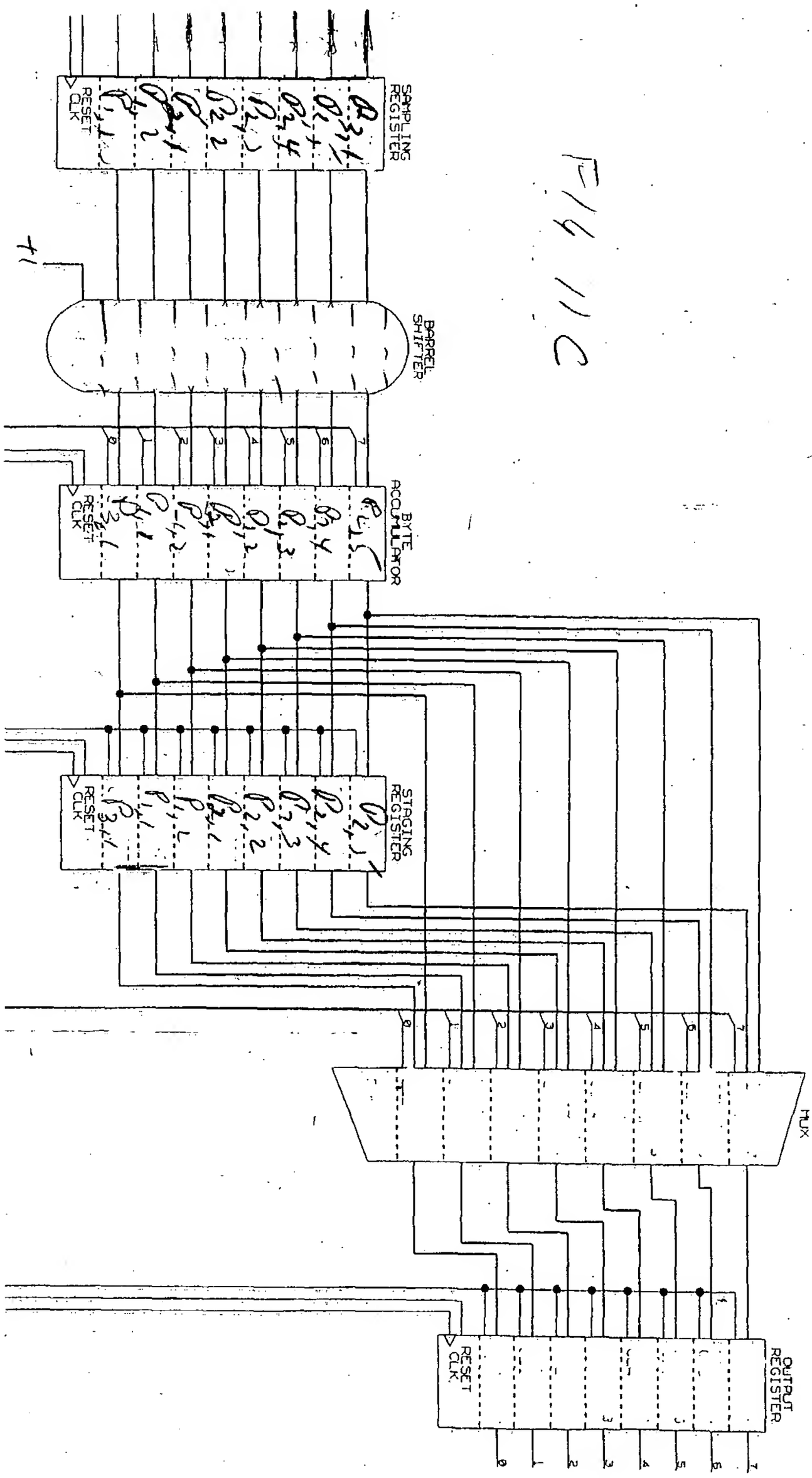

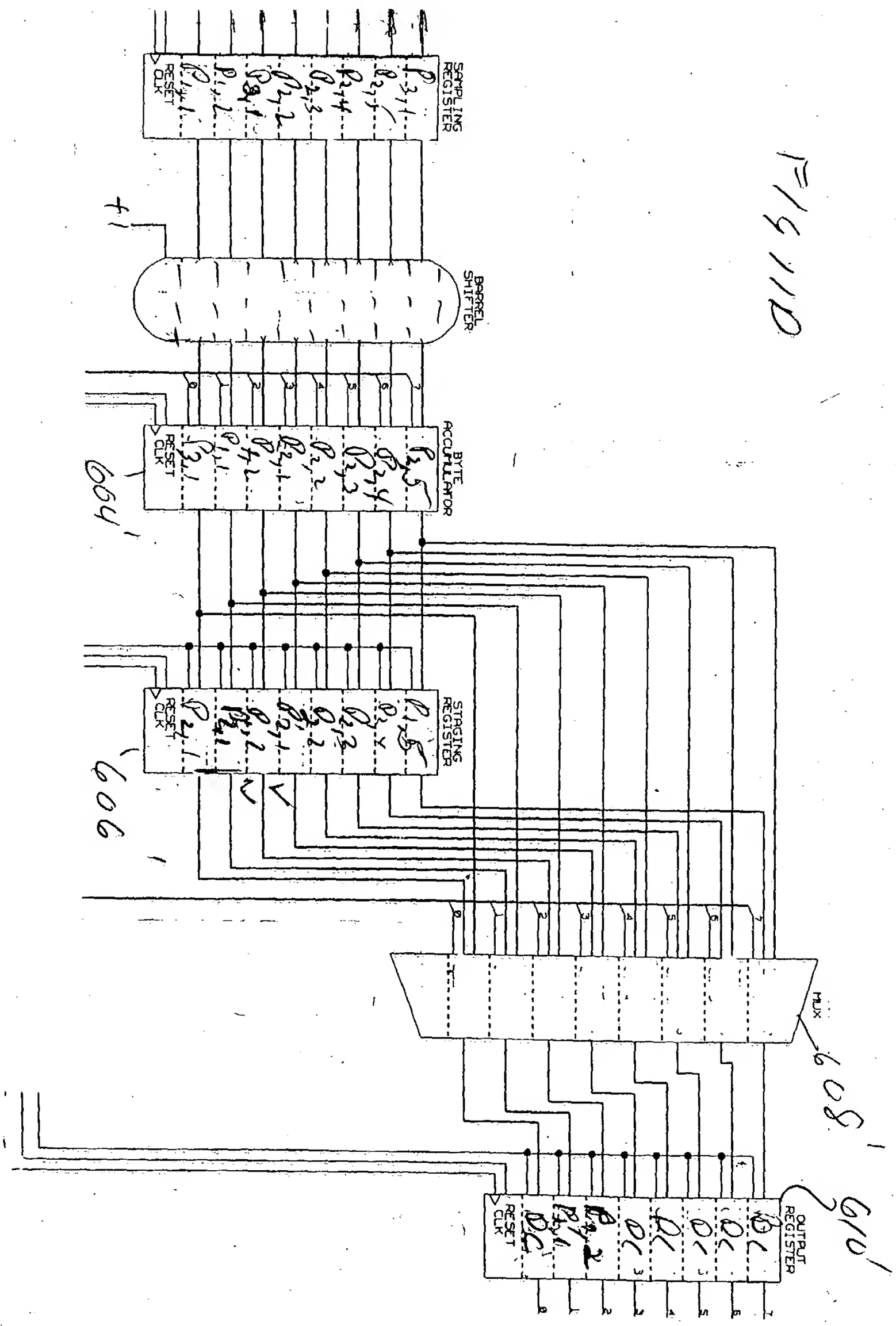
SAMPLING REGISTER
RESET CLK
+1
BARREL SHIFTER
BYTE ACCUMULATOR
STAGING REGISTER
MUX
OUTPUT REGISTER
604
606
608
610

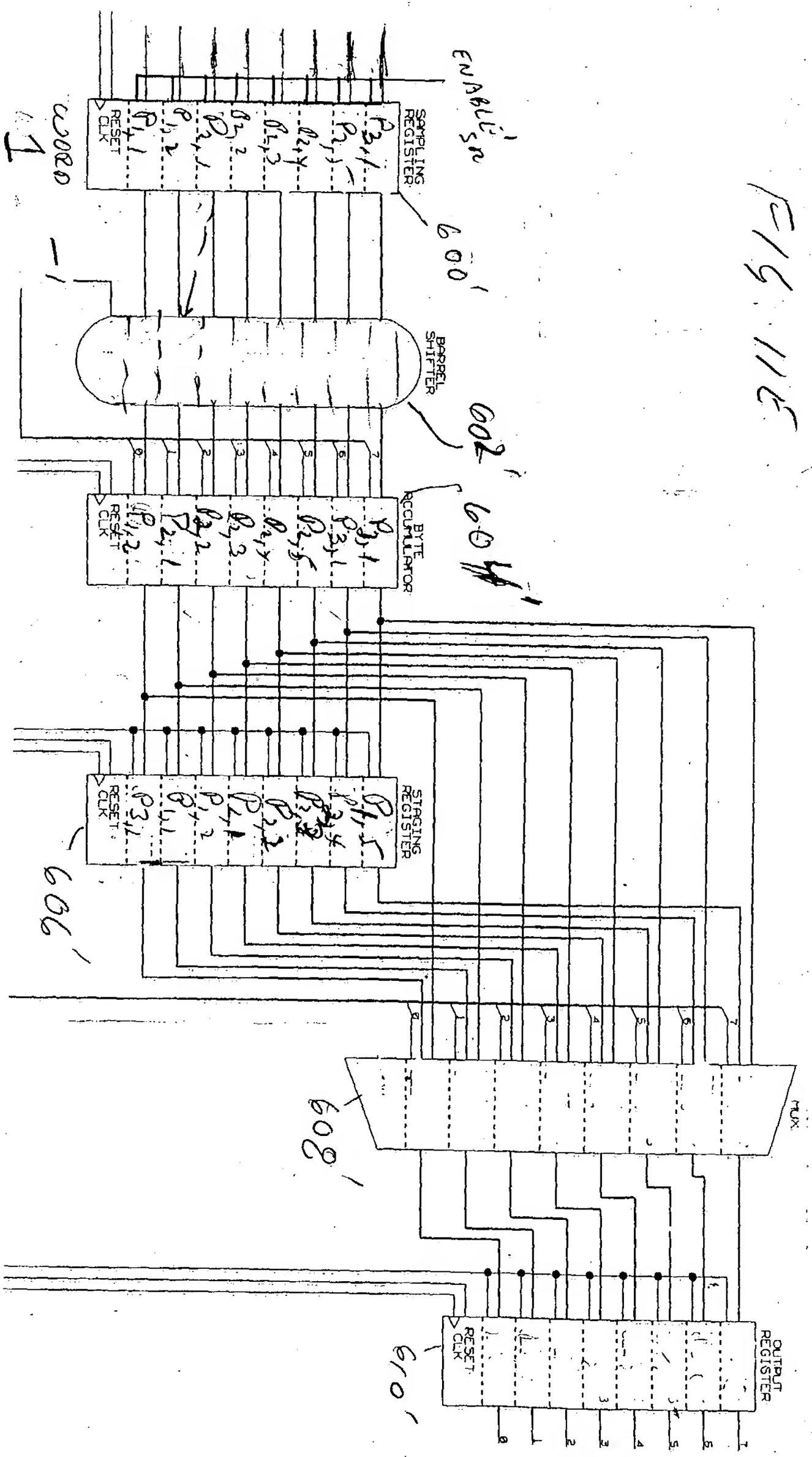
RESET
CLK
SAMPLING REGISTER
ENABLE
600
BARREL SHIFTER
602
BYTE ACCUMULATOR
604
STAGING REGISTER
606
MUX
608
OUTPUT REGISTER
610

Fig. 11E

DATA STORAGE SYSTEM PACKER/UNPACKER
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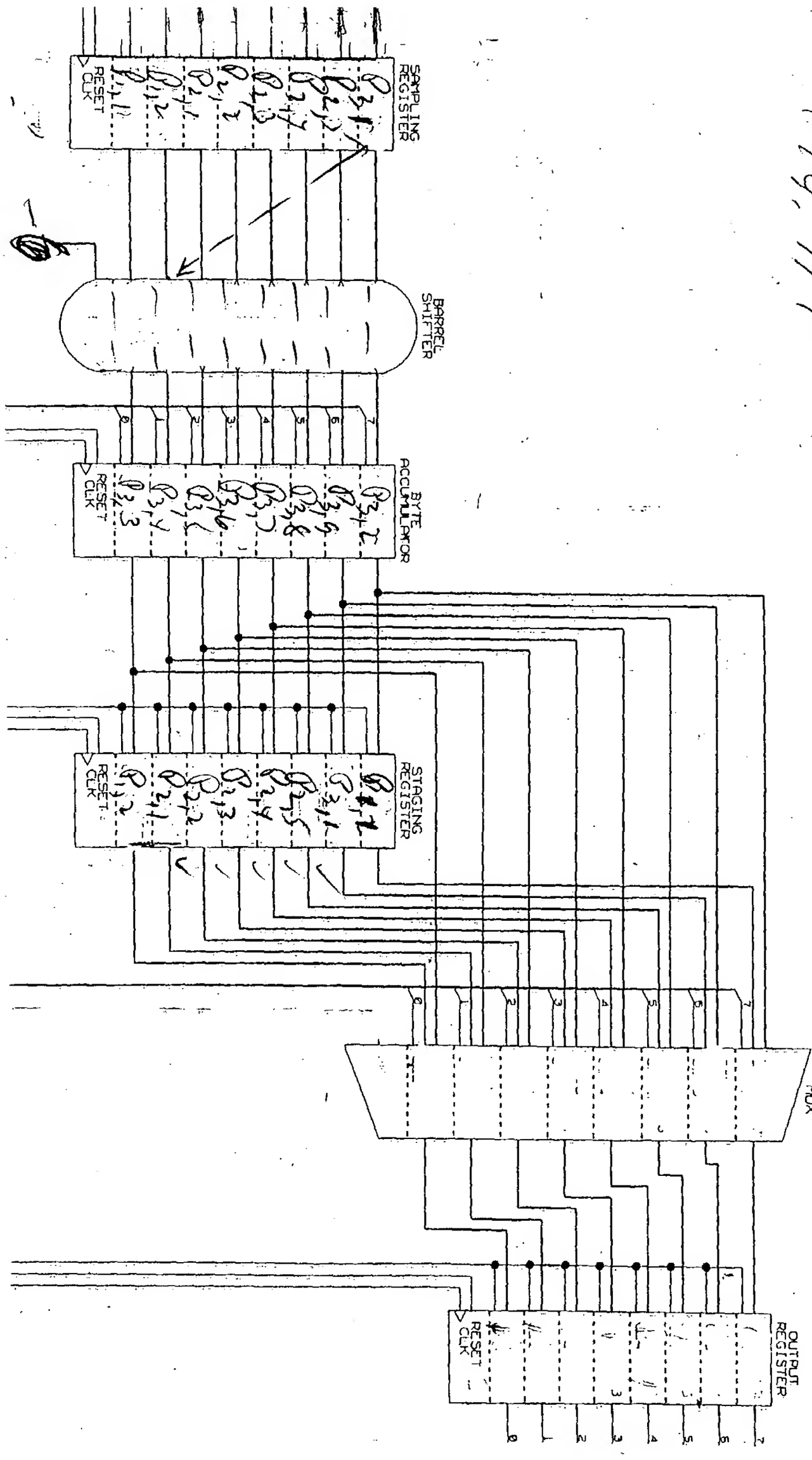

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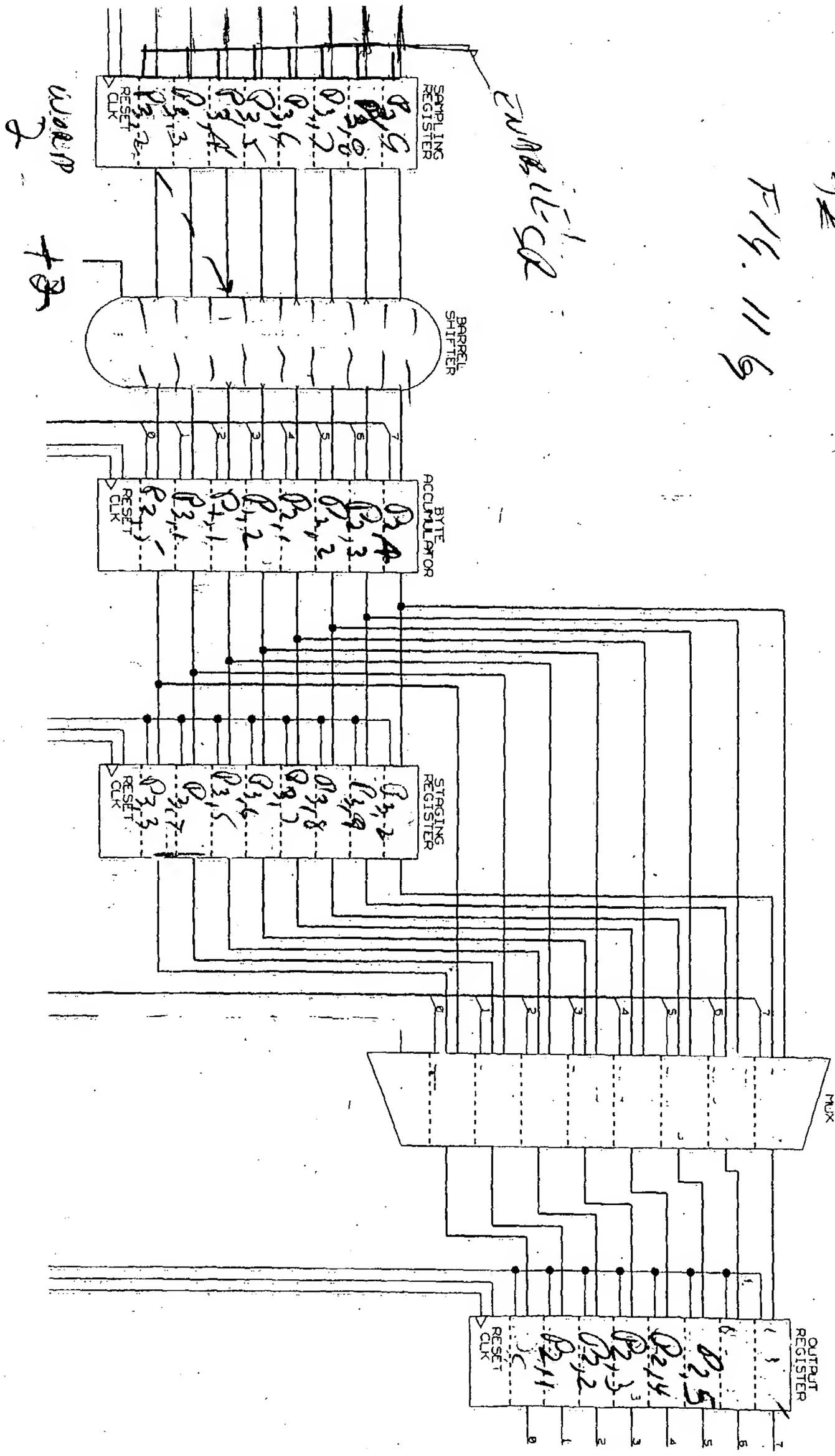

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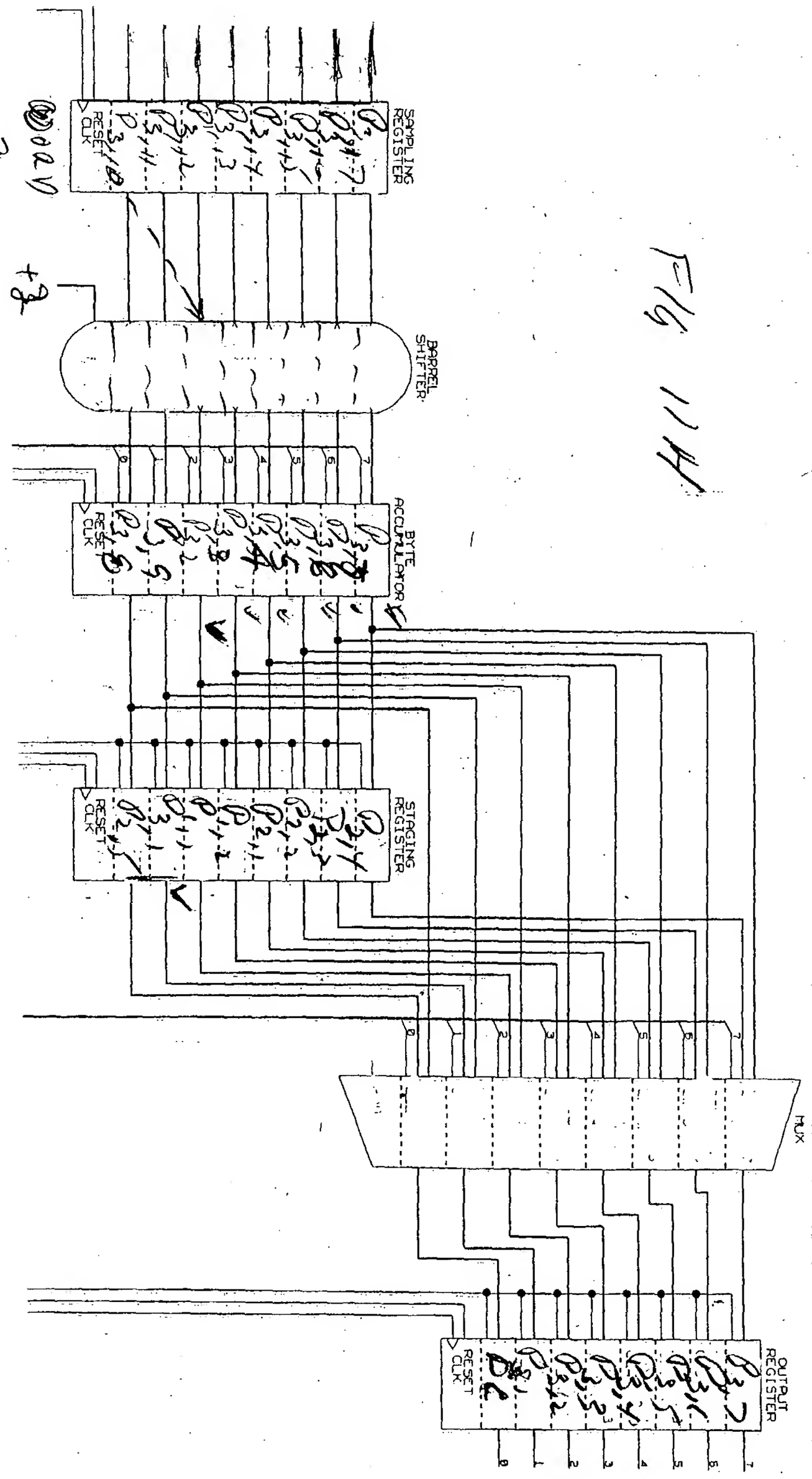

Fig 11A

DATA STORAGE SYSTEM PACKER/UNPACKER
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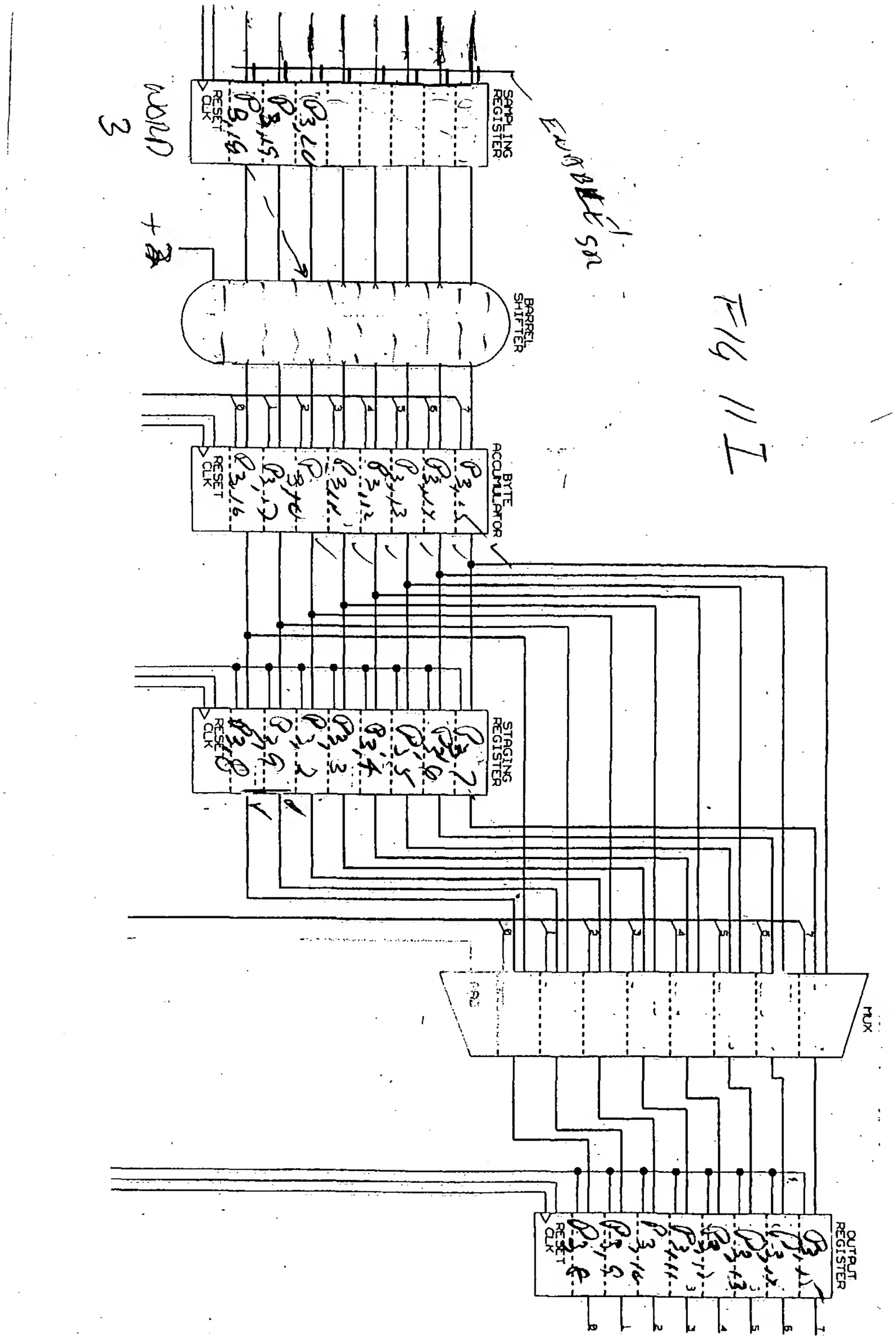
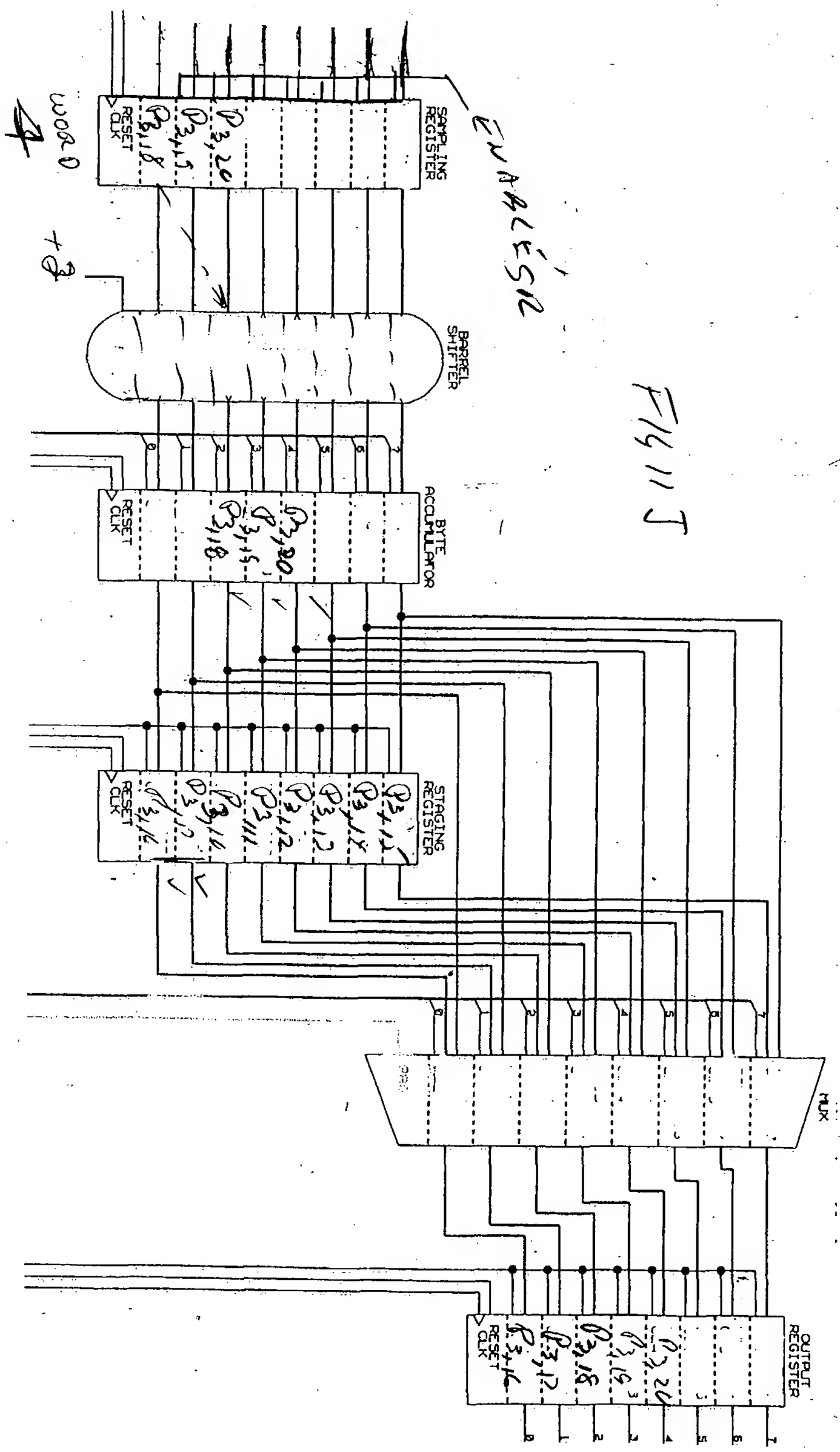


FIG 11 I

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